Evaluation of IGBT thermo-sensitive electrical parameters under different dissipation conditions – Comparison with infrared measurements

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Abstract

Junction temperature evaluation is a key parameter used to control a power module assembly. But measuring the junction temperature by thermo-sensitive electrical parameters (TSEPs) does not reveal the actual temperature of the semiconductor device. In this paper, a specific electronic board used to compare four common TSEPs of single IGBT chip is presented. For this comparison, two dissipation modes are used: dissipation in active and saturation regions. In order to have referential measurements we carried out surface temperature measurements of IGBT chip with an infrared (IR) camera. A dedicated numerical tool is presented to estimate the mean surface temperature of active region. The comparison between IR and TSEP measurements shows that the best studied parameter (in terms of robustness and usability) is the gate emitter voltage for single chip temperature evaluation.

Keywords
IGBT, thermo-sensitive parameter, infrared measurements, thermal characterization

1. Introduction

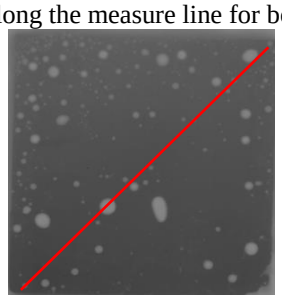
The junction temperature T_j measurement of a power semiconductor device can be used to characterize the thermal performances of its package and as a damage indicator of the power module assembly (principally for the detection of a delaminating process) [1]. Three main methods are currently used to evaluate the junction temperature of power semiconductor devices [2]: optical methods, physical contact methods and electrical methods.

Although optical and physical contact methods can be very accurate, they require generally an intrusive modification of the power module (e.g. remove the gel…). Furthermore, the measurement time cannot generally be shorter than 1ms due to the electronic treatment or to the thermal capacitance of thermo-sensitive tools. Nevertheless, some specific optical methods have been developed to permit a high time resolution for only single component without power packaging [3-5]. This is why the junction temperature is commonly measured using a thermo-sensitive electrical parameter (TSEP): the chip itself is the temperature sensor. Several TSEPs can be used for the chip temperature evaluation under operating conditions [6-9]. They will not be discussed in this paper. Other TSEPs are dedicated to the measurement of thermal resistances or impedances of power modules and to the study of their aging. They are mainly used by power devices manufacturers.

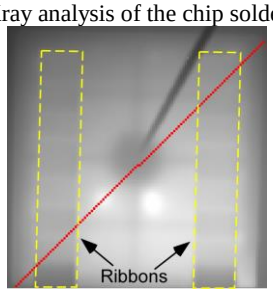
However, the accuracy obtained using these TSEPs is debatable. Indeed, the chip temperature being very non-homogeneous, the junction temperature value given by a TSEP lies between the maximum and minimum temperatures. Therefore large junction temperature differences can be obtained using different techniques. For power MOSFETs in TO220 packages, Jakopovic et al. [10] demonstrate that the measured thermal resistance can vary from 0.9K/W using the channel resistance as a TSEP, to 1.25K/W using the threshold voltage, i.e. a 28% difference. To get a better evaluation of the junction temperature value given by the collector-emitter voltage $V_{ce,sat}$ using the low current method, Schmidt and Scheuermann [11] compare it with the temperature map given by an IR camera. In their experiment, they demonstrate that the junction temperature given by this TSEP (108.5°C) is very close to the average surface temperature (106.3°C).

In their paper, Jakopovic et al. [10] also show that the temperature measured by a TSEP is largely dependent on the dissipation mode. In fact, they compare the thermal impedances obtained with dissipations in saturation region and in active region. A 20% difference is estimated between the two measurements. However, the authors do not give any referential temperature measurements in order to validate their results.

In the case of an IGBT chip, dissipation in saturation region is obtained when the collector current value I_c is regulated by a power supply and the gate-emitter voltage V_{ge} is close to 15V. Dissipation in active region is obtained when the chip operates in its amplification region, i.e. V_{ce} is largely higher than the saturation voltage and is fixed by a power supply, I_c is regulated acting on the V_{ge} voltage. As an illustration of the effect of the dissipation mode, Fig. 1 shows, on the left, an IR image of a dissipating IGBT (in active region) and an X-ray analysis of the chip solder. In this example, the electrical connexions on the chip are made with ribbons. On the right, the temperature is plotted along the measure line for both dissipation modes with a dissipated power close to 94W.



Xray analysis of the chip solder



IR measurement of the IGBT which operate in active region (measure line in red)

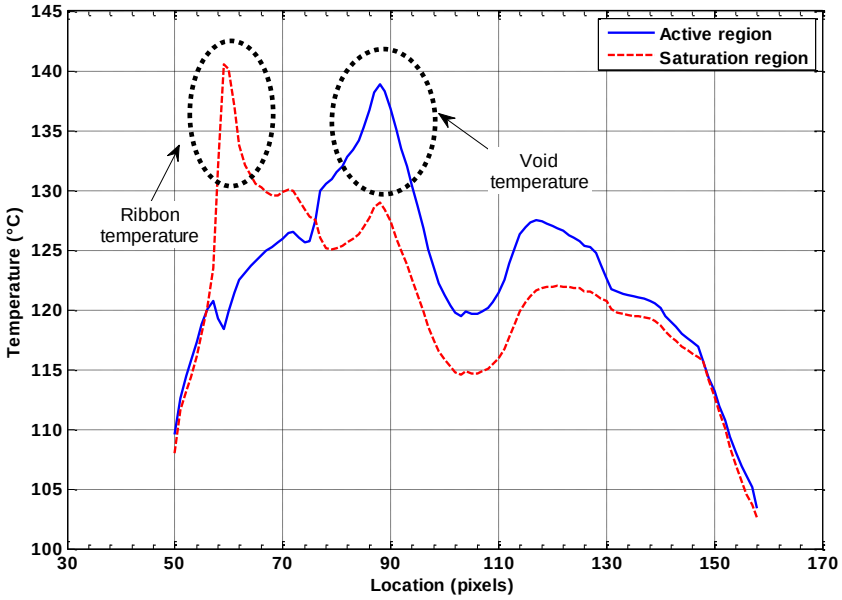


Fig. 1. Comparison of IR measurements for dissipations in active and saturation region (P close to 94W)

We can see in Fig. 1 that for dissipation in saturation region, the ribbons are hotter than the IGBT chip. This is due to the high current value (close to 80A). For dissipation in active region, joule heating is reduced due to the lower current level (5A) and the ribbon temperature is very close to the silicon chip temperature. Near the center of the IGBT chip, we can see a temperature elevation due to a void in the solder. The location of this void is correlated with the X-Ray analysis. When dissipating in active region, we can see that the temperature variation due to the void is higher. In the right side of this graph, we can see that temperature variations in other areas are also higher. The difference between the temperature maps in active and saturation regions is mainly due to electro-thermal effects that change the current repartition on the surface of the chip and that are different in each dissipation mode. For example, in the case of dissipation in active region, the current density is higher in hotter areas because a temperature growth induces a reduction of the threshold voltage.

In this paper we propose to provide complementary results for IGBT chip temperature evaluation with TSEPs. We will use an infrared camera (FLIR SC7500) as a referential chip temperature measurement to compare the temperature map of a dissipating IGBT die with the junction temperature given by four common TSEPs. The first one is the measurement of the collector-emitter voltage under a low collector current. It will be called $V_{ce,sat}$. This is a very common TSEP, used for all power devices like IGBTs, MOSFETs or diodes [12-14]. The low current value makes it possible to obtain measurements with negligible self-heating of the device. The second TSEP is the threshold voltage V_{th}. It is used with MOSFET or IGBT chips and is generally determined with a very low current regulation acting on the gate voltage [15,16]. The third TSEP is the gate-emitter voltage under a high current I_c. The measurement principle is identical to that of the V_{th} measurement, but the collector current and the collector-emitter voltage are high enough to induce self-heating of the device [17]. This TSEP is called $V_{ge,I}$. The last TSEP is the saturation current I_{css}. It can be used with IGBT or MOSFET chips. For this measurement, the gate-emitter (or gate-source) voltage value is slightly higher than the threshold voltage V_{th} of the device [18]. A current probe measures the resulting saturation current.

For each TSEP, we will measure the temperature under two different dissipation conditions:

-dissipation in saturation region (full conduction, V_{ge}=15V),

-dissipation in active region.

In the first part of this paper, we will present the experimental setup, i.e. the studied power module, the test bench, and an electronic board that was developed for this study. Then we will present the numerical tool used to estimate the mean surface temperature of the IGBT active part using IR measurements. In the following section, all TSEPs are described, and we give their dependence with temperature. Finally, IR measurements are compared to chip temperature measurements obtained with each TSEP. Using these results, we compare all TSEPs in terms of robustness and usability.

2. Experimental setup

2.1. Description of the power modules

The studied transistor chips are 600V-200A INFINEON IGBTs (SIGC100T60R3). Their thickness is 70µm. All test campaigns were carried out with a simplified power assembly (Fig. 2). Each transistor chip (T_1 and T_2) is soldered on a 1.5mm thin copper substrate. The IGBT power electrical connections (emitter and collector) are made with aluminum ribbons. The gate connection is realized with wire bonding. The power module is opened and the dielectric gel is removed so as to allow IR measurement of the chip surface temperature. Black paint is deposited on the module surface so as to control the emissivity ε of the surface (ε > 0.94).

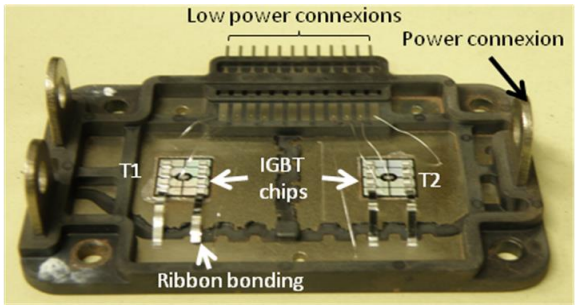


Fig. 2. The tested power module

The power module is mounted on a cold plate (Fig. 3). The electrical insulation between each copper plate and the thermal contacts between each part is provided by a thermal interface material (Denka BFG30A). A 3 mm thick aluminum plate is inserted between the module and the cold plate. Two holes are machined so as to make temperature measurements with thermocouples located under each chip center. These thermocouples give a temperature value that makes it possible to calculate the thermal resistance between each dissipating IGBT chip and the aluminum plate (section 6).

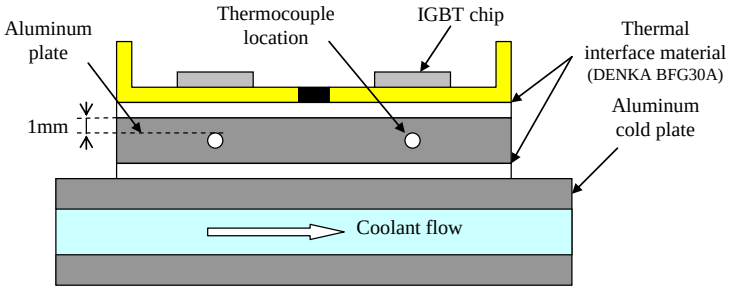


Fig. 3. Cross section of the power module on the cold plate

2.2. Test bench

The test bench is developed around an infrared camera mounted on a manual positioning solution. The temperature of the device undergoing testing is controlled from 20°C to 180°C by the cold plate connected to a temperature control instrument (Julabo Presto). All electrical measurements are made with a Dewetron data acquisition system (DEWETRON: DEWE5000). The voltage accuracy of this system is ±0.04% of reading plus ±0.05% of range (DEWETRON: DAQP-LV differential voltage amplifier). All measurements are isolated from each other, and the bandwidth is 300kHz. A specific electronic circuit has been developed to compare the different TSEPs. This circuit is driven by a Labview program and an NI USB-6259 board connected to a computer.

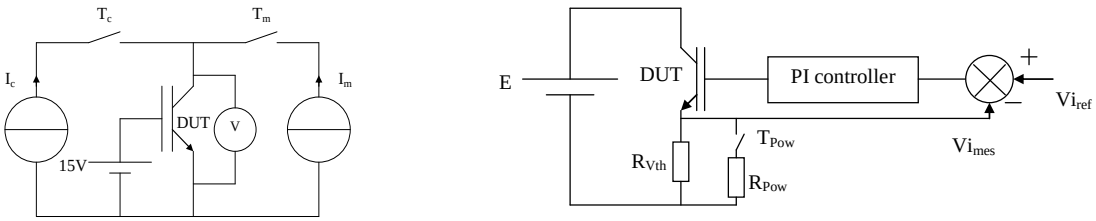
3. Principle of chip temperature measurements by different TSEPs

3.1. Measurement aims

The measurement of a chip temperature with a TSEP is always made in two steps [2]. In the first one, the TSEP is calibrated as a function of temperature. In the second, called dissipation step, the chip is crossed by a relatively high current so as to create self-heating and then measure the junction temperature.

For example, the use of $V_{ce,sat}$ as a TSEP is generally made using the method shown in Fig. 4.a [14][19]. For calibration, the switch T_c is off and T_m is on. I_m is a low current (between a few mA and a few hundred mA) so as to keep self-heating of the device negligible. The IGBT temperature is varied using an external heating system, so as to measure $V_{ce,sat}$ as a function of temperature. During dissipation, T_c is on and T_m is off in order to increase the junction temperature using a high current I_c. After temperature stabilization, the current is reduced to a lower value I_m (T_m on and T_c off). The temperature decrease can then be directly deduced from this measurement using the $V_{ce,sat}(T_j)$ curve obtained during calibration [2]. The initial temperature value can be estimated by extrapolation and can be used to calculate the steady-state temperature at the end of the dissipation step [2]. For such a measurement, we notice that the IGBT chip is used in saturation region (full conduction – V_{ge}=15V) when it dissipates.

For a temperature measurement with V_{th} as a TSEP, the calibration step can be made with a very low current regulation acting on the gate-emitter voltage. The current value is a few mA so as to work as close as possible to the actual threshold voltage and to limit self-heating of the device. The current regulation can be made automatically using a low current source and connecting together the gate and collector electrodes of the device. It can also be made using a control loop with, for example, a PI controller. This is the solution chosen by Cao et al. [20] (Fig. 4.b). They carry out calibration by controlling the voltage across R_{Vth} and keeping the switch T_{Pow} off. For the dissipation step, T_{Pow} is on. R_{Pow} is much lower than R_{Vth} so as to substantially increase the IGBT current and thus the junction temperature. For the temperature measurement, T_{Pow} is open and the temperature is deduced from the $V_{th}(T_j)$ curve obtained during the calibration step. During dissipation the IGBT is used in active region because E is generally higher than $V_{ce,sat}$.



a. $V_{ce,sat}$ as TSEP b. V_{th} as TSEP

Fig. 4. Different methods for carrying out chip temperature measurements

From these examples, we can see that the dissipation mode of an IGBT is often linked to the TSEP chosen for the thermal study of the package. We have demonstrated that $V_{ce,sat}$ is used as a TSEP with dissipation in saturation region. For V_{th} [20] and $V_{ge,I}$ [17] measurements, the IGBT generally works in active region. For I_{css}, Ayadi et al. [21] present a solution using dissipation in saturation region. As said above, the temperature distribution in the chip is different when dissipating in active or saturation regions. This could be one reason why Jakopovic et al. [10] obtained large differences when measuring a MOSFET thermal resistance using different dissipation modes. In other words, it was clearly worthwhile comparing the results given by each TSEP using each dissipation mode for IGBTs. We therefore decided to create a specific electronic board to make measurements associating all TSEPs with all dissipation modes. This will be outlined in the following section.

3.2. Description of the electronic board

In order to compare all TSEPs, we have developed a specific experimental and configurable test bench (Fig. 5). It has been designed to have three dissipation modes in the IGBT (DUT): one in saturation region (V_{ge}=15V) and two in active region (V_{ge}=V_{ce} or I_c controlled under a given V_{ce}). The configuration of the different measurements and power dissipation modes is carried out using 7 switches (T_1 to T_7). All switches are driven by a Labview program.

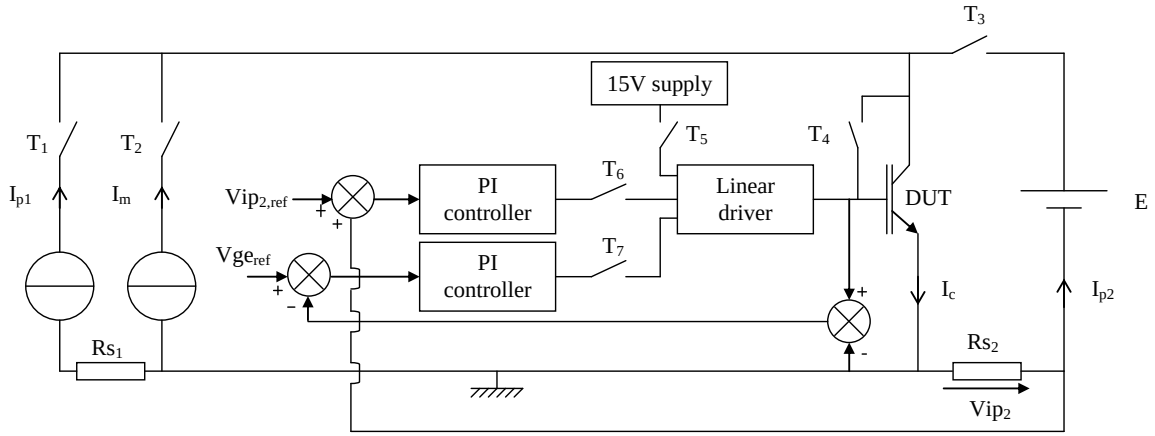


Fig. 5. Description of the electronic circuit

3.2.1. Calibration

$V_{ce,sat}$ is measured by applying a gate-emitter voltage V_{ge}=15V on the IGBT (T5 on). The current I_c is created by the current source I_m=50 mA (T2 on). All other switches are off.

V_{th} is measured by injecting a fixed current I_c=I_m=50mA (T2 on). For this measurement, the gate electrode is connected with the collector electrode i.e. V_{ce}=V_{ge} (T4 on). All other switches are off.

$V_{ge,I}$ is measured with a current control loop including a PI controller (T6 on). For this measurement, the IGBT chip is fed by a voltage supply E (T3 on). The current value I_c=I_{p2}=5A is chosen so as to work in active region. All other switches are off.

The saturation current I_{css} is measured with a V_{ge} control loop (T3 and T7 on, others off). The value of V_{ge} has to be higher than the threshold voltage of the device. In our test, V_{ge} equals 6.4V, so as to have a current value I_{p2} high enough to obtain accurate measurements with the shunt resistor Rs_2=10mΩ. The regulation loop was used to avoid voltage oscillations during the measurements.

All the calibration measurements are taken during a short time adjustable from 20µs to 1000µs, so as to avoid substantial self-heating of the chip especially when using $V_{ge,I}$ or I_{css} as a TSEP.

3.2.2. Dissipation

As previously explained, dissipation can be produced in different working regions of the power device. For dissipation in saturation region, T_5 and T_1 are on. I_c is measured with a shunt resistor Rs_1. In active region, two solutions were studied:

- $V_{ce}=V_{ge}$ where T_1 and T_4 are on: the current is imposed by a power supply and is measured with Rs_1 ;
- $V_{ce}=E$ where T_3 and T_6 are on: the current is fixed by the control loop and is measured with Rs_2.

The dissipation level in saturation region and in active region ($V_{ce}=V_{ge}$) is controlled acting on the I_{c1}value (45A, 60A and 75A in saturation region and 6A, 9A and 12A in active region). In the other case (dissipation in active region with $V_{ce}=E$), the collector current I_c equals 5A and is regulated acting on the gate-emitter voltage. The variation of the power is thus made acting on the V_{ce} value (10V, 15V and 20V). The maximum power level being about 100 W due to the value of the thermal resistance of this power module, the I_c value was chosen in order to work with voltage levels largely higher than the saturation voltage ($V_{ce}\geq 10V$).

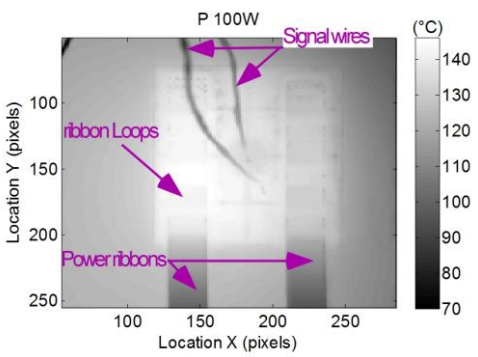
Table 1
States of the switches for the different measurements and dissipation modes

		T_1	T_2	T_3	T_4	T_5	T_6	T_7
Calibration	$V_{ce,sat}$	off	On	off	off	on	off	off
	V_{th}	off	On	off	on	off	off	off
	$V_{ge,I}$	off	Off	on	off	off	on	off
	I_{css}	off	Off	on	off	off	off	on
Dissipation	Saturation	on	Off	off	off	on	off	off
	$V_{ge}=V_{ce}$	on	Off	off	on	off	off	off
	$V_{ce}=E$	off	Off	on	off	off	on	off

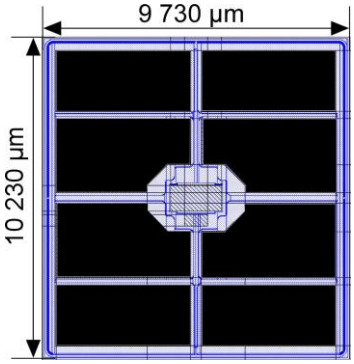
In order to compare the chip temperatures obtained with this electronic circuit and with IR measurements, we have developed a method for obtaining an accurate chip surface temperature with an IR camera. It is presented below.

4. Calculation of the surface temperature

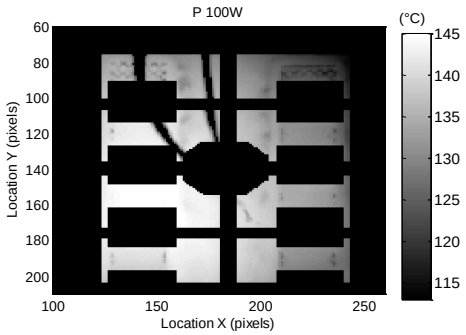
As mentioned in section 2, the IGBT power electrical connections are made with ribbons. They have been chosen because the area viewed by the IR camera is larger than the area obtained with wire bonding technology [11]. Fig. 6.a presents an example of the temperature distribution on a 100 W dissipating IGBT. With this temperature map, we are able to evaluate the mean surface temperature of the device active part. This temperature will be used as a referential measurement and compared with temperatures obtained using each TSEP (section 6). After each IR measurement during calibration and power dissipation, the temperature of the IGBT chip is estimated. To obtain an accurate temperature value, we recorded 100 images (100 Hz frequency) and then calculated the mean temperature of each point of the temperature map. A top view of the chip can be seen in Fig. 6.b, with the active parts shown in black. A Matlab program was developed to extract the useful junction temperature. A numerical mask was used to specifically exclude the electric connections and inactive areas of the IGBT chip. In Fig. 6.c the black areas show the temperature zones which are excluded for the temperature calculation. Then the top surface chip temperature distribution was extrapolated with the help of local bilinear fitting adjustments, so as to estimate the temperature under the electrical connections (Fig. 6.d). The surface temperature calculation is described in details in [22].



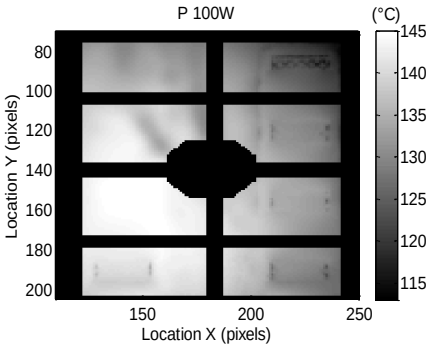
a. Temperature distribution on a dissipating IGBT



b. IGBT chip presentation



c. Temperature measurement with a numerical mask



d. Reconstructed chip surface temperature

Fig. 6. Principle of the IR measurements

5. Calibration results

In this section we will outline the calibration procedure and the measurement conditions for all TSEPs. Then we will show their dependence as a function of temperature. Due to convection and radiation heat transfers between the module and its environment, the chip temperature is lower than the cold plate temperature. Thus it was estimated using the IR camera. The procedure presented in section 4 was used to evaluate the mean temperature of the IGBT active part. This temperature was considered to be the chip temperature.

5.1. Collector-emitter voltage $V_{ce,sat}$ under a low collector current I_c=50mA

This TSEP is measured as a function of temperature and for both IGBTs (T_1 and T_2) in the module (Fig. 7). We can see that the variation of this parameter is almost linear with temperature. The sensitivity is about -2.3mV/°C for a 50mA current injection. We can also see that results provided for both IGBTs are very close to each other. Linearity and reproducibility make this TSEP very popular for temperature measurements. The current level was chosen in order to have a linear variation of this TSEP. If the current value was too low, this TSEP could be nonlinear [23]. The dissipated power is lower than 25mW and does not induce any observable self-heating during the short calibration time (500µs).

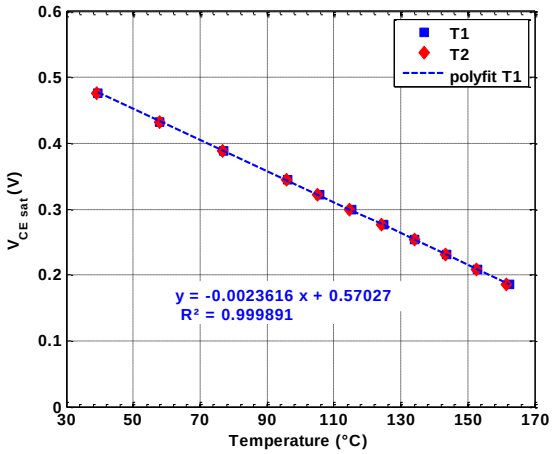


Fig. 7. $V_{ce,sat}$ as a function of temperature (IGBT T_1 and T_2)

5.2. Threshold voltage V_{th} (I_c=50mA)

V_{th} is measured as a function of temperature and for each IGBT (Fig. 8). The variation of this parameter is not linear. In fact, sensitivity increases from -9.5mV/°C for low temperatures to -13mV/°C for high temperatures. A second order polynomial fitting seems to give a good approximation of this parameter with temperature. We can also see that this TSEP varies from one chip to another in the same power module. An accurate temperature measurement therefore requires a calibration of each die. The current level has to be high enough in order to have a quadratic variation of this TSEP [23], this is why we have chosen 50mA. The dissipated power during the calibration time (500µs) is lower than 350mW and induces a very negligible self-heating of the IGBT (no voltage variation is observed during the calibration time).

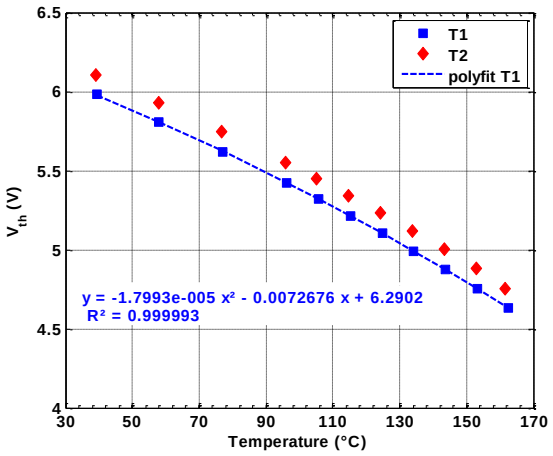


Fig. 8. V_{th} as a function of temperature (IGBT T_1 and T_2)

5.3. The gate-emitter voltage $V_{ge,I}$ under a high current

$V_{ge,I}$ is measured when T_3 and T_6 are on (Fig. 9). As stated above, the collector current I_c is fixed by a control loop acting on the gate-emitter voltage V_{ge}. The minimum V_{ce} value (10V) was chosen in order to be higher than the saturation voltage. In our experiments (section 6), the minimum dissipated power being close to 50W, I_c equals 5A.

We define t_1 as the time corresponding to a current I_c equal to the final current value divided by two (here 2.5A). In this measurement, the dissipated power in the chip (V_{ce}*I_c) induces non negligible self-heating. In order to visualize this self-heating, we show the zoomed evolution of V_{ge} with time in Fig. 10. We can see that V_{ge} decreases by about 10mV in 400µs. We will see later that a V_{ge} decrease clearly shows an elevation of the junction temperature. In order to measure the $V_{ge,I}$ value before self-heating, we first establish an interpolation curve of $V_{ge}(t)$. Because of the low temperature variation during the measurement time, we can use a linear interpolation as a function of the square root of time [2,20]. The value of $V_{ge,I}$ is then estimated by calculating the value of the interpolation curve when $t=t_1$.

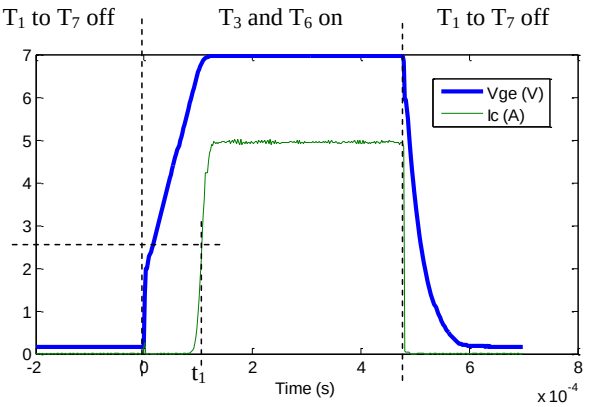


Fig. 9. Measurement of $V_{ge,I}$ (cold plate temperature 40°C and E=20V)

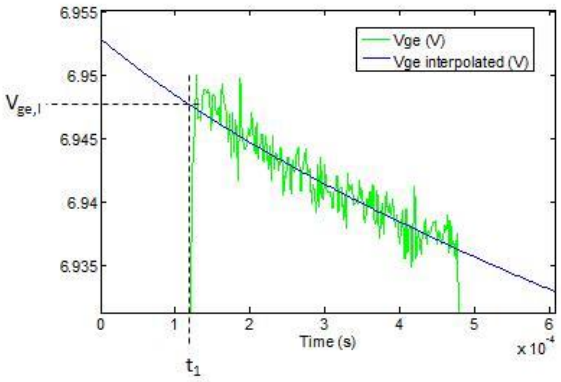


Fig. 10. Self-heating and interpolation of V_{ge} (cold plate temperature 40°C and E=20V)

Fig. 11 shows $V_{ge,I}$ as a function of temperature for different V_{ce} values of the IGBT T_1. As in the case of V_{th}, the curves can be extrapolated by a second order polynomial function. In this case, sensitivity varies as a function of temperature between -6mV/°C for low temperatures and -7.5mV/°C for higher temperatures. We can conclude that V_{th} is a better TSEP because its sensitivity is higher and the absolute measured voltage value is lower. The temperature measurement can therefore be more accurate. We can also see in Fig. 11 that this TSEP does not substantially depend on the V_{ce} value. For example, the difference between $V_{ge,I}$ given at 40°C using V_{ce}=10V and V_{ce}=25V is only 12mV. The error is thus close to only 2°C. As for V_{th}, this TSEP gives different values if we use T_2 instead of T_1. A calibration procedure of all transistors in a power module is thus also required.

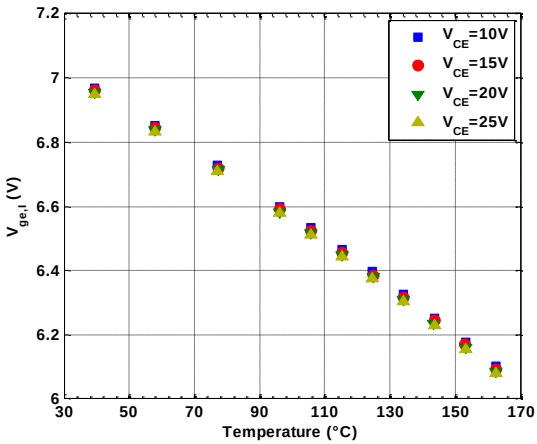


Fig. 11. $V_{ge,I}$ as a function of temperature with different V_{ce}=E values (IGBT T_1)

5.4. The saturation current I_{css}

As in the case of $V_{ge,I}$, there is self-heating during the measurement. To obtain an accurate value of this TSEP, we again used an interpolation method. Fig. 12 shows that this TSEP is not linear and depends substantially on the transistor chip. The choice of V_{ge}=6.4V was made considering two opposite constraints:

- for lower temperatures, the current is low and the 10mΩ shunt voltage have to be high enough to have accurate measurements. The minimal current was estimated to be close to 2A.
- for higher temperatures, the current becomes high and creates a very high instantaneous power and thus a large increase of the chip temperature during the measurement.

Due to these constraints, we have not measured this TSEP in the whole temperature range because the accuracy was poor for low temperatures. Indeed, the current being very low (shunt voltage lower than 20mV), the signal was very noisy.

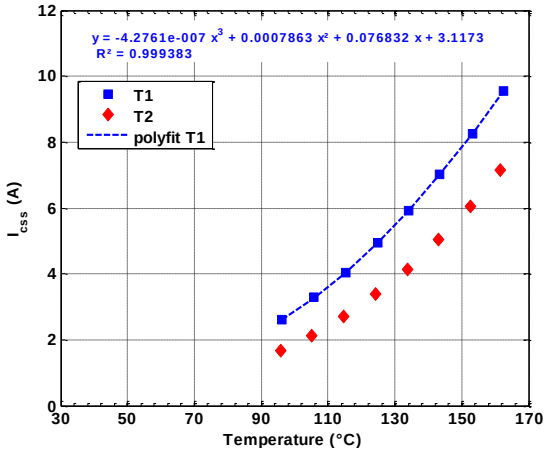


Fig. 12. I_{css} as a function of temperature with V_{ce}=25V

6. Temperature measurements

6.1. Measurement principle

Temperature measurement is carried out in four steps. First, the chip dissipates to induce self-heating. We wait for the temperature to stabilize so as to be in steady state conditions: temperature visualization is done using the IR temperature map of the device. As mentioned above, dissipation can be made in active or saturation regions. Second, the Labview program opens all switches. It introduces a short delay time (several tens of µs). Then, in the third step, the TSEP is measured to estimate the chip temperature. The duration of this step is a few hundred µs. Finally, in the last step, all switches are opened.

Fig. 13 describes the sequence of different stages for the temperature measurement. In this example, dissipation is made in active region with V_{ce}=E (I_c control acting on the gate-emitter voltage). The TSEP is I_{css}. We can see that before -20µs, the chip is dissipating. Then a delay time is introduced by opening all switches. After this delay time, measurement of I_{css} is carried out.

Note that the temperature measurements have to be taken with care. Above all, the chip cools down after the beginning of the delay time, introducing a variation of the measured electrical parameter. It is thus necessary to estimate the parameter value at the end of the dissipation step so as to obtain the chip temperature during dissipation. To measure V_{th} and $V_{ce,sat}$, the chip temperature measurement can easily be carried out using an extrapolation curve, as suggested by a number of authors [2, 20]. For $V_{ge,I}$ and I_{css}, the calculation is more difficult. In fact, during the measurement of the electrical parameter, a dissipated power exists. Therefore, considering that the rising time of the current I_c is short, three dissipation powers exist during the temperature measurement: $P=P_{steady\text{-}state}$ before the delay time, P=0W during the delay time and the establishment time of the current (t_1 in Fig. 13), and $P=P_{measure}$ between t_1 and the end of the measurement. Thus the chip temperature is estimated in two steps: in the first one, we calculate the temperature decrease ΔT between the beginning of the delay time and t_1. Then an extrapolation method gives the temperature $T(t_1)$. The chip temperature is then calculated as $T_{chip}=T(t_1)+\Delta T$.

For the measurement of ΔT, we have to use complementary results given by TSEPs having a negligible dissipated power: V_{th} or $V_{ce,sat}$. Using the cooling curves obtained with these TSEPs, it is possible to estimate the value of the temperature difference ΔT between the end of the dissipation and t_1. In the case of dissipation in active

region, we use V_{th} which seems the more accurate TSEP (§6.2.2). In the case of dissipation in saturation region, we use $V_{ce,sat}$ (§6.2.4). In our measurements, the maximum value of ΔT is 1°C which is not a negligible value. It is due to the delay time (<380µs) introduced by our regulation loops which are not optimized.

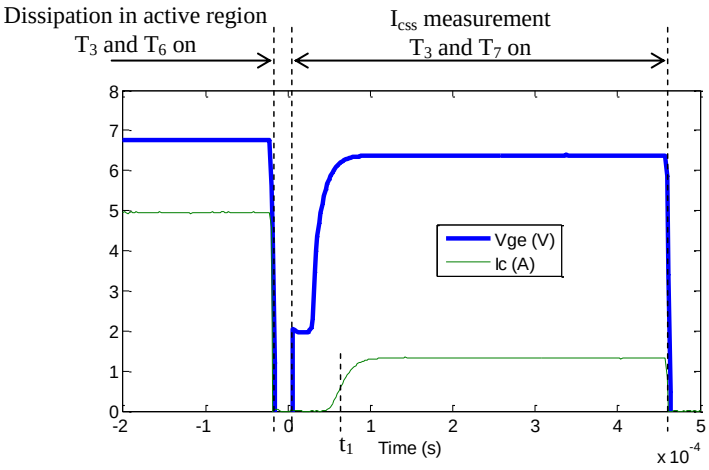


Fig. 13. Example of a chip temperature measurement with I_{css} as TSEP and dissipation in active region

6.2. Results

6.2.1. Introduction

To compare the different results, thermal resistances are preferred to chip temperatures because the cold plate temperature varies a little (by a few °C) during the tests. Furthermore it is not simple to keep a constant dissipating power. As described in section 2.1., two thermocouples are used to measure the temperature in the aluminum base plate under the module. With this data the thermal resistance between each IGBT chip and this base plate can be calculated. The thermal resistance obtained with each TSEP (Rth_{TSEP}) will be compared with the one obtained by IR measurements (Rth_{IR}). These values are calculated using the following equations:

$$Rth_{IR} = \frac{T_{mean,IR} - T_{thermo}}{P} \quad (1)$$

$$Rth_{TSEP} = \frac{T_{TSEP} - T_{thermo}}{P} \quad (2)$$

where $T_{mean,IR}$, T_{TSEP}, T_{thermo} and P are respectively the mean temperature obtained by IR measurements, the temperature given by each TSEP, the thermocouple temperature and the power dissipated by the chip. For each dissipation mode, we compare the results given by all TSEPs and IR measurements using the Rth_{ERROR} indicator calculated with the following equation:

$$Rth_{ERROR} = \frac{Rth_{TSEP} - Rth_{IR}}{Rth_{IR}} \quad (3)$$

6.2.2. Dissipation in active region (V_{ce}=E)

Table 2 gives results for chip temperatures and thermal resistances obtained during the characterization campaign. Three dissipated power levels were chosen to compare three temperature values keeping a quasi-constant cold plate temperature. Measurements have been carried out with both IGBT chips T_1 and T_2. The last column gives the percentage error between the thermal resistance calculated with the TSEP and the one estimated with the IR mean surface temperature. For V_{th} and $V_{ge,I}$ as a TSEP, this error is relatively low for both IGBTs. It appears to increase with the dissipated power but stays below 4.5%. The corresponding temperature difference is <1°C when P is about 46W, and <3°C when P is about 95W. We can also see that the chip temperature measured by these TSEPs is always higher than the mean surface temperature. I_{css} gives high errors for lower powers. That is normal because this TSEP was not calibrated for these temperature levels. For other power levels, I_{css} gives good results with errors lower than 4%. The most surprising results are those given by $V_{ce,sat}$. In contrast to other measurements, the temperature given by this TSEP is always lower than the mean surface temperature. The error is very high for lower powers: 18%. The corresponding temperature difference is about 6°C for low powers and 4°C for high powers.

The temperature difference measured using $V_{ce,sat}$ could be explained by the localization of the dissipation area in the thickness of the die. In fact, when working in active region, the power is mainly dissipated in the front side of the die i.e. in the channel and in the top junction. Because the heat flux goes from the top of the die to the substrate, the backside of the IGBT is logically colder than the front side. $V_{ce,sat}$ measuring the temperature of the junction in the backside, the result seems to be logical. However, the thickness of the die is only 70µm. If we assume that the dissipation on the top side is uniform, the thermal resistance of the chip is close to $5*10^{-3}$K/W inducing a temperature gradient equals to 0.25°C from the top to the back side if the dissipation power is 50W. The higher temperature difference observed during the measurements could be explained by the fact that the current distribution in the front side is not uniform because it is principally located in the channel. This non uniformity creates high temperature gradients near the channel. The decrease of the temperature gradient when growing the power level could be explained by a better repartition of the current in the top side when increasing the voltage level. This better repartition is due to the increase of the current in the junction located at the top side of the die. However, this analysis has to be confirmed by electro-thermal modelling in further works.

Table 2
Results with dissipation in active region and V_{ce}=E

TSEP	P (W)	T_{thermo} (°C)	IGBT	T_{TSEP} (°C)	Rth $_{TSEP}$ (K/W)	$T_{mean, IR}$ (°C)	Rth $_{IR}$ (K/W)	Rth $_{ERROR}$ (%)
$V_{ce,sat}$	46.09	38.42	T1	65.80	0.59	71.90	0.73	-18.2
V_{th}	46.28	38.93	T1	73.38	0.74	72.62	0.73	2.3
$V_{ge,I}$	46.27	38.92	T1	73.41	0.75	72.58	0.73	2.5
I_{css}	46.28	38.94	T1	75.72	0.79	72.56	0.73	9.4
$V_{ce,sat}$	70.66	48.12	T1	94.50	0.66	99.72	0.73	-10.1
V_{th}	70.68	48.13	T1	101.52	0.76	99.82	0.73	3.3
$V_{ge,I}$	70.67	48.11	T1	101.42	0.75	99.82	0.73	3.1
I_{css}	70.65	48.12	T1	101.59	0.76	99.81	0.73	3.5
$V_{ce,sat}$	94.99	56.92	T1	122.64	0.69	126.55	0.73	-5.6
V_{th}	95.00	57.33	T1	129.84	0.76	126.79	0.73	4.4
$V_{ge,I}$	95.02	57.31	T1	129.15	0.76	126.79	0.73	3.4
I_{css}	95.02	57.32	T1	129.59	0.76	126.98	0.73	3.8
$V_{ce,sat}$	45.12	37.11	T2	67.24	0.67	73.52	0.81	-17.3
V_{th}	45.17	37.71	T2	74.91	0.82	74.27	0.81	1.7
$V_{ge,I}$	45.16	37.72	T2	75.42	0.83	74.21	0.81	3.3
I_{css}	45.16	37.02	T2	78.58	0.92	73.60	0.81	13.6
$V_{ce,sat}$	69.50	46.09	T2	95.85	0.72	101.30	0.79	-9.9
V_{th}	69.54	46.30	T2	103.15	0.82	101.75	0.80	2.5
$V_{ge,I}$	69.55	46.50	T2	103.88	0.82	101.90	0.80	3.6
I_{css}	69.57	46.50	T2	103.54	0.82	102.02	0.80	2.7
$V_{ce,sat}$	93.86	54.89	T2	124.81	0.74	129.28	0.79	-6.0
V_{th}	93.84	55.29	T2	131.92	0.82	129.56	0.79	3.2
$V_{ge,I}$	93.89	55.29	T2	132.34	0.82	129.57	0.79	3.7
I_{css}	93.97	55.28	T2	131.43	0.81	129.62	0.79	2.4

6.2.3. Dissipation in active region ($V_{ce}=V_{ge}$)

The same tests have been carried out with dissipation in active region and $V_{ce}=V_{ge}$. The results are so similar to those shown in table 2 that we will not present a separate table for them here. The same problem is observed with the use of $V_{ce,sat}$. For I_{css} (under normal conditions) and $V_{ge,I}$, the error is always lower than 3.5%..

6.2.4. Dissipation in saturation region

Table 3 gives the results obtained with dissipation in saturation region for IGBT T_2. The results obtained with T_1 are similar. By contrast to previous tests, $V_{ce,sat}$ gives good results. The error between this TSEP and IR measurements stays below 3%. The corresponding temperature difference is lower than 1.5°C. In saturation region, the power losses are located in the junction of the backside, in the drift region and in the top side (channel + top junction). Therefore the dissipation is more uniform than in the case of dissipation in active region. This could explain why the results are

very close each other using all TSEPs. This has to be confirmed by complementary electro-thermal studies. When the chip temperature is correct, I_{css} and $V_{ge,I}$ also give good results (error < 1.5%).

Table 3
Results with dissipation in saturation region

TSEP	P (W)	T_{thermo} (°C)	IGBT	T_{TSEP} (°C)	Rth_{TSEP} (K/W)	$T_{mean\ IR}$ (°C)	Rth_{IR} (K/W)	Rth_{ERROR} (%)
$V_{ce,sat}$	45.30	37.11	T2	74.35	0.82	73.88	0.81	1.3
V_{th}	45.16	36.83	T2	NA	NA	73.13	0.80	NA
$V_{ge,I}$	44.93	37.12	T2	74.66	0.84	74.09	0.82	1.5
I_{css}	45.11	37.12	T2	76.96	1.97	74.13	0.82	7.7
$V_{ce,sat}$	69.38	45.22	T2	101.85	0.82	100.45	0.80	2.5
V_{th}	69.50	44.81	T2	NA	NA	99.59	0.79	NA
$V_{ge,I}$	69.04	45.62	T2	101.17	0.80	100.73	0.80	0.8
I_{css}	69.74	45.71	T2	101.13	0.79	100.83	0.79	0.5
$V_{ce,sat}$	93.86	53.80	T2	127.59	0.79	126.99	0.78	0.8
V_{th}	94.02	53.71	T2	NA	NA	126.41	0.77	NA
$V_{ge,I}$	94.15	54.20	T2	127.97	0.78	127.28	0.78	0.9
I_{css}	93.71	54.21	T2	127.47	0.78	127.33	0.78	0.2

Chip temperatures obtained with V_{th} are not included in the table because the measurements were not satisfactory. In fact, first measurements gave results with large temperature errors (higher than 10°C). In order to understand the problem, we have increased the duration of the calibration time from 500µs to 1ms. Fig. 14 shows the shape of $V_{ge}(t)$ during the measurement time. We have observed a sudden change in the V_{ge} value for times higher than 500µs. After this change, the value of V_{ge} gives temperature results very close to these obtained with other TSEPs. We think that this problem is due to the charge of parasitic capacitances of power switches in the electronic circuit. We have chosen not to use the V_{th} results because the extrapolation method should produce large measurement errors under these conditions.

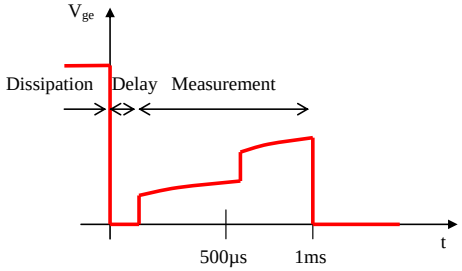


Fig. 14. Measurement of V_{th} with dissipation in saturation region

6.3. Discussion

6.3.1. Effect of the dissipation mode

As said above, the difference between both dissipation modes is principally due the location of the dissipation areas in the chip. First, the repartition is not the same in the thickness of the die. In the case of dissipation in active region, this phenomena induces a lower temperature in the bottom junction and therefore an underestimation of the temperature using $V_{ce,sat}$ as a TSEP. Second, the repartition of the dissipated power is different on the surface of the chip because of the non-uniformity of the current density which is due to electro-thermal effects. As said above the use of dissipation in active region seems to increase the temperature variations on the chip surface (Fig. 1).
However the effect of the dissipation mode cannot be observed clearly using $T_{mean\ IR}$. In fact, Table 2 and Table 3 show that the thermal resistance measured with the IR camera seems to be nearly identical in active and saturation regions. On the contrary, $V_{ge,I}$ and I_{css} used as TSEPs give higher thermal resistances in active region. For dissipation power close to 94W, the thermal resistance difference is about 2%. Since the sensitivity of these TSEPs increases with temperature, they are more sensitive to temperature variations. That could confirm that surface temperature variations are higher for dissipation in active region (see Fig. 1).

Because of the higher temperature variations, we think that the dissipation in active region could be very helpful

for studying some aging damage in the backside of the chip because emerging defaults like solder delamination could be observed earlier compared with a classical dissipation in saturation region. In a first approach, we can suppose that in the case of dissipation in active region, the fixed V_{ge} induces a dependence of the apparent local electrical impedance due to the local threshold voltage of IGBT cells that trends to increase the current density where the temperature is higher. We can therefore suppose that dissipation in active region allows a better visualization of the down packaging layers defaults like chip solder voids.

6.3.2. Choice of a TSEP

$V_{ce,sat}$ is currently the most used TSEP. This is due to several reasons:
- it is presented as the most accurate TSEP used in power electronics [23],
- the negligible self-heating during its measurement allows a very simple characterization process,
- the measuring time can be very short (tens of µs) unlike $V_{ge,I}$ or I_{css} that necessitate a regulation loop (section 5).

However, examination of the results presented in this paper shows that it sometimes produces high errors, especially for dissipation in active region. By contrast, I_{css} and $V_{ge,I}$ give very good results in all dissipation modes. The case of V_{th} is different. In fact, measurements could not be carried out when dissipating in saturation region. This is probably due to our experimental setup; we think that such a measurement might be possible. Our study can therefore not conclude on the use of this TSEP in all dissipation modes. However, we can confirm that it can be used with interest when dissipating in active region. Results are generally very close to those given by $V_{ge,I}$. An important conclusion of this work is that I_{css} and $V_{ge,I}$ are the most robust TSEPs because they can be used in all dissipation cases with low temperature and thermal resistance errors.

Both I_{css} and $V_{ge,I}$ could easily be used to measure chip temperatures and thermal resistances. For the measurement of a thermal impedance Z_{th}, $V_{ge,I}$ is the most convenient parameter because the dissipating power is naturally constant: the collector current I_c is controlled (and therefore is constant) and V_{ce} is given by the voltage source (and is also constant). By contrast with measurements with $V_{ce,sat}$ and V_{th}, Z_{th} can be measured when the power device heats up and not when it cools down. I_{css} can hardly be used for the Z_{th} measurement because V_{ce} is given by a voltage source while I_c depends on the temperature. This leads to a time dependence of the dissipated power and therefore to a difficult thermal impedance measurement.

Finally this work proves that, in the case of a single IGBT chip, the most robust and convenient TSEP is the gate-emitter voltage $V_{ge,I}$ under a high current I_c even if complementary modeling and experimental studies will need to be carried out so as to generalize this result.

7. Conclusion

In this paper, we proposed an experimental setup to compare the IGBT chip temperature measured with an IR camera and with four TSEPs ($V_{ce,sat}$, V_{th}, $V_{ge,I}$ and I_{css}). For this comparison, we constructed a dedicated electronic board which enabled us to measure the chip temperature using all these TSEPs and two different dissipation conditions (in active and saturation regions). We also developed a numerical tool to estimate the mean IR surface temperature of an IGBT chip. This tool consists of masking the non active parts of the silicon chip and estimating the temperature of parts which are hidden by electrical connections. Then we studied the evolution of all TSEPs with temperature.

Finally, we compared the results given by each TSEP and the IR camera in terms of thermal resistance. For $V_{ge,I}$ and I_{css}, a very good correlation was obtained between IR and TSEP measurements in all dissipation conditions. Problems were identified when using $V_{ce,sat}$ in active region and V_{th} in saturation region. The measurement of $V_{ce,sat}$ gave thermal resistances different from those obtained with IR measurements (up to 20%). It was not possible to measure V_{th} in active region with our electronic board. $V_{ge,I}$ seems to be the best TSEP because it is robust and can easily be used to measure a thermal impedance.

Note that this paper is a first step to improve our knowledge of indirect chip temperature measurements using TSEPs. This work has to be completed in order to help power electronics engineers when they choose a TSEP for a given application. In fact, this work was only dedicated to single IGBTs without ageing considerations. Because a power switch is generally composed with several IGBT chips, a TSEP evaluation of two paralleled IGBTs has been presented in [22]. In this case, the dissipation in active region is not possible because the current is not the same in both chips: the current density is largely higher in the chip having the smallest threshold voltage. In another part of our future works, an evaluation of the ageing effects on TSEPs robustness will be carried out. In this case, the TSEP ageing itself need to be evaluated. A correlation with main ageing damages in conventional power modules (power connections, metallization, gate oxide…) have also to be studied. At this time, a first evaluation on the power wire bonding lift off impact has been initiated and will be presented in a future paper.

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